Cancellation of third order Intermodulation currents in a two-stages amplifier topology.

Sébastien Dardenne[1,2], Claude Duvanaud[2], Frédéric Robin[1], Francis Huin[1], Jean-Marie Paillot[2], Rachid Allam[2]

[1] ACCO S.A, 21 bis rue d'Hennemont, 78100 St-Germain-en-Laye – France.

[2] LAII-UPRES-EA1219, Université de Poitiers, 4 Av de Varsovie, 16021 Angoulême – France.

Abstract — **This paper gives a detailed description of a linearization technique using a two-stages amplifier. The first stage is used to generate third order intermodulation products (IMD3), which will be added to the input signal of the second stage in order to cancel the IMD3 at its output. The technique effectively improves the linearity of the system. To investigate the effect of IMD3 injection, analytical calculations of the drain currents for the fundamental frequencies f_1 and f_2 and for the third order intermodulation currents $2f_1$-f_2 and $2f_2$-f_1 are established without and with injection of intermodulation components at the input of the power stage. To evaluate the improvement provided by the proposed technique, a two-tone test at carrier frequency of 900 MHz is performed with a MESFET GaAs. The test procedure is described and measurements show a great improvement of IMD3. A Carrier to third intemodulation ratio C/I3 of 55dBc was achieved for a 19 dBm output power, compared with 25 dBc achieved without the first stage.**

I. Introduction

The power amplifier (PA) is one of the key components in mobile communication handsets determining the power consumption and, thus, the battery life of the handsets. To decrease electrical consumption and improve power efficiency, the amplifier must be used in its saturation zone. In such a mode, amplitude and phase distortions are important.

In order to accommodate high bite rate, linearity and multimode/multiband capability are being highlighted as the most significant issues of power amplifiers. Efficient modulation techniques in term of spectral efficiency have been adopted and have inevitably non-constant envelope, therefore, power amplifiers with high linearity are required in the transmitter system. [1]

Predistorsion techniques [2] have already been studied and developed because they avoid disadvantages of feedback techniques encountered at RF and microwave frequencies. They are generally designed with series or shunt diodes [3][4] or transistors [5]. The non-linearity of the device is used to modify signal amplitude and phase in opposition with AM-AM and AM-PM distortions of the power amplifier. Generally, their introduction in the transmitter causes an insertion loss and consequently, a decrease of the gain of the complete system.

In this communication, the use of a two-stages amplifier is proposed; the particular operation of a first stage is presented in order to cancel IMD3 at the output of the second stage, the power stage. The aim of this work is to show that the IMD3 at the output of a power stage can be reduced by applying IMD3 components at its input with appropriate amplitude and phase.

In a first part is presented a study of the drain current components at the output of a power amplifier versus an input signal composed of two carriers and two IMD3 components. In a second part, circuit description, test measurements and results of a two-stages amplifier topology are exposed.

II. Expression Of The Drain Currents

The principle of the proposed technique is illustrated on Fig. 1 for a two tones excitation signal and in the case of the application of IMD. The aim of this analysis is to demonstrate that the injection of IMD components at the input of a transistor can lead to a compensation of output IMD.

By applying two carriers f_1 and f_2 of same amplitude and phase at the input of a power amplifier, its non-linearity will produce intermodulation frequencies at $2f_1$-f_2 and $2f_2$-f_1.

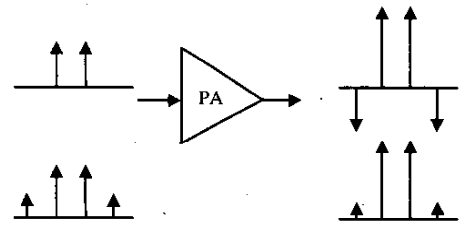

Fig. 1. Two different input signals and output due to non-linearity of the PA.

0-7803-7695-1/03/$17.00 © 2003 IEEE

The excitation signal is now taken as two unmodulated carriers at f_1 and f_2 of equal amplitude A and two carriers at $2f_1-f_2$ and $2f_2-f_1$ of equal amplitude B. By changing the sign of B, the IMD3 component can be in phase or out of phase with the fundamental component. Its expression is:

$$V_{gs}(t)=A.\cos(\omega_1.t)+A.\cos(\omega_2.t) +B.\cos[(2\omega_1-\omega_2).t]+B.\cos[(2\omega_2-\omega_1).t] \quad (1)$$

The study assumes that the drain to source current Ids is the most critical component to the non-linear behaviour of the device. Drain-source current in a MESFET is controlled by the gate-source and drain-source potentials, V_{gs} and V_{ds}. A third-order representation [6] of small-signal drain current $I_{ds}(V_{gs},V_{ds})$ can be expressed by a two dimensional Taylor's series as :

$$I_{ds}(V_{gs},V_{ds})=G_m.V_{gs}+G_{m_2}.V_{gs}^2+G_{m_3}V_{gs}^3+G_d.V_{ds} \quad (2)$$

Gm, Gm_2 and Gm_3 are respectively the transconductance and the derivatives of Gm with respect to V_{gs}. Gd is the drain to source conductance.

The drain voltage depends on the load presented to the drain current source at each frequency component. The analysis assumes that the same load R is presented to the drain source in the full bandwidth; moreover, drain voltage components at low and harmonic frequencies are short-circuited.

With the previous expression of drain current (2) and excitation signal (1), the following expressions of the drain current components can be achieved :

$$I_{d|f_1,f_2}=\frac{1}{1+R.G_d}.(G_m.A+\frac{9}{4}.G_{m_3}.A^3 +\frac{9}{2}.G_{m_3}.A.B^2+\frac{9}{4}.G_{m_3}.A^2.B) \quad (3)$$

$$I_{d|2f_1-f_2,2f_2-f_1}=\frac{1}{1+R.G_d}.(\frac{3}{4}.G_{m_3}.A^3 +G_m.B+\frac{9}{2}.G_{m_3}.A^2.B+\frac{9}{4}.G_{m_3}.B^3) \quad (4)$$

Fig. 2 shows the variations of the calculated IMD3 currents (equation(4)) for a transistor biased in class AB soft (Vgs=-1,8V) for four values of B. For B equal to 0, the IMD3 current is negative and decreases according to the increase of the input level. For positive values of B, we can see that the IMD3 current is equal to 0 for different values of A. Those points correspond to the cancellation of IMD3 at the output of the power stage.

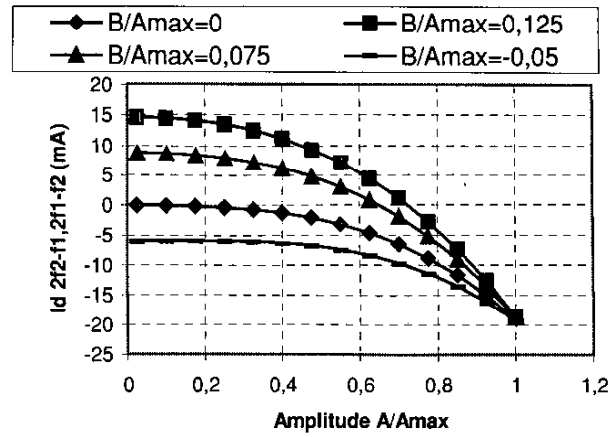

Fig. 2. Simulated IMD3 currents at the output of the power stage without and with injection of IMD3 components at its input

This result shows that cancellation of the output IMD3 currents can be achieved by an appropriate adjustment of the IMD3 voltage applied at the input. Furthermore, for a bias voltage V_{gs}=-1.8V of the power stage, the suitable value of B is positive to cancel output IMD3 currents; thus, it means that the signals at $2\omega_1-\omega_2$, and $2\omega_2-\omega_1$ have to be in phase with the fundamental carriers at ω_1 and ω_2.

III. Generation Of Positive IMD3 Currents

As illustrated in equation (4), the sign of the IMD3 currents depends directly of the sign of Gm_3 [6]. From the previous calculation, the device is biased at Vgs=–1,8V (class AB soft) and the corresponding value of Gm_3 is negative, resulting in a negative IMD3 currents.

The following part proposes to analyse the sign of Gm_3 with respect to the gate bias voltage.

For a fixed value of the drain voltage Vdd, the third derivative of the measured Ids with respect to Vgs gives the coefficient Gm_3. Its variation is plotted on Fig. 3. Near pinch off, Gm_3 is positive, and then becomes negative and closed to –1V, it becomes positive again. So it is possible to generate positive or negative IMD3 current.

The bias condition of the transistor gives us the sign of the IMD3 current. For a class B biased transistor, IMD3 currents will be positive; if the bias voltage rises up to a class A, then the IMD3 current component becomes negative.

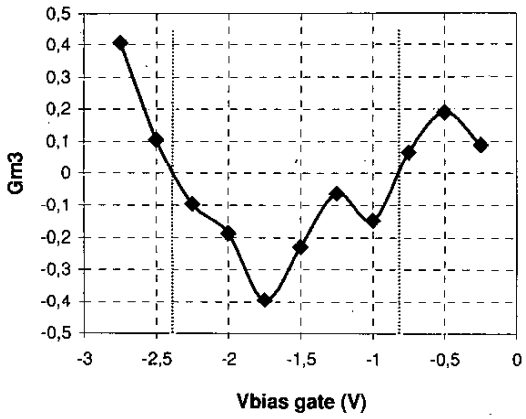

Fig. 3. Variation of Gm3 with respect to the gate bias voltage at fixed value of Vdd=3V.

The IMD3 variations are quite different between small and large signal excitation. The previous model, based on a truncated series, does not take into account saturation effects. Under large signal excitation, those effects must be considered.

A non-linear simulator is used to establish the condition of cancellation of the IMD3 drain currents. Performances have been simulated in Harmonic Balance using the ADS simulator. (Fig. 4)

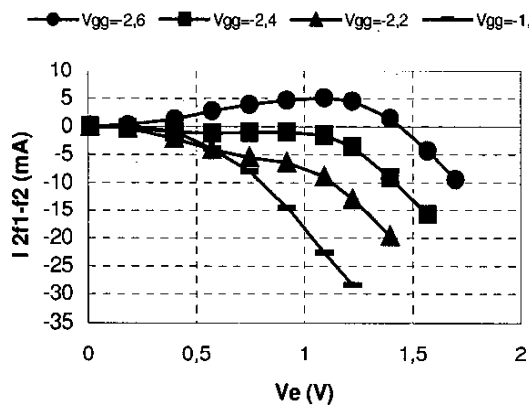

Fig. 4. Simulated intermodulation currents versus input level for different bias levels and for a pinch-off voltage of –2,6V.

We obtained the following behaviour : In class A, the IMD3 currents are negative and decrease with respect to the increase of the input signal level. If the bias level is set to a class B, the IMD3 currents become positive up to a peak value, then decrease and change their sign. This behaviour is due at low level to the sign change of Gm_3 versus biasing and at high level to the drain current saturation.

The proposed design is composed of two transistors used with different bias. The first one will be used in class B, generating positive IMD3 currents which will cancel the IMD3 currents generated by the second stage amplifier used in class AB.

IV. Experimental Results

Fig. 5 shows the basic block diagram for test setup. The input signal is composed of two carriers f_1 and f_2 of same amplitude. A directionnal coupler at the output of the first stage allows to measure the power of the IMD3 added to the input signal of second stage. To demonstrate that a cancellation of IMD3 can be achieved by injecting IMD3 components, a given output level has been selected and maintained for all measurements (19 dBm). Different gate biases are used to modify the IMD3 generated by the first stage. For each bias voltage, input level and the attenuator value are adjusted to have the same power level.

This procedure allows to achieve different IMD3 power levels for the same fundamental frequency power level at the output of the first stage.

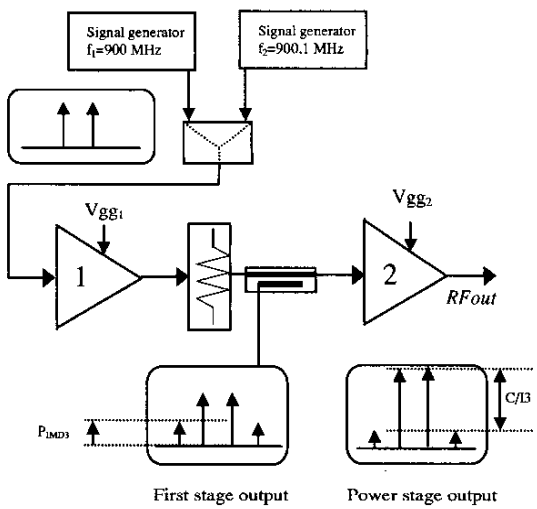

Fig. 5. Block diagram of test setup

Fig. 6 shows test measurements obtained for a fixed output power of +19dBm at carrier frequencies of 900MHz and 900.1MHz. These results show that by varying the operating parameters of the first stage, it is possible to generate IMD3 currents so that they cancel those at the output of the second stage. A C/I3 peak was observed for a gate bias voltage of –2,5V. The second curve of the Fig. 6 shows the IMD3 power at the output of the first stage. We can notice that the C/I3 peak of the second stage does not occur when the IMD3 power at the output of the first stage is minimum.

For a gate bias voltage of –2,4V, the minimum IMD3 power of the first stage is achieved. This point corresponds to the change of sign of IMD3. At this point, the first stage does not generate any IMD3 currents and the C/I of the global amplifier is equal to 25 dBc. For lower gate bias voltages, IMD3 currents are positive and an optimum value allows reducing the IMD3 at the output of the second stage; At this point, a C/I3 of 55 dBc is achieved. For larger gate bias voltages, IMD3 currents are negative and degrade linearity.

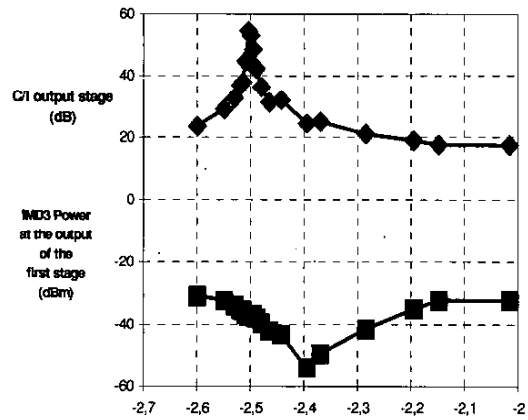

Fig. 6. Measured second stage C/I3 and first stage IMD3 power versus gate bias voltage of the first stage.

V. CONCLUSION

An IMD compensation technique using a two-stages amplifier was proposed in detail. Non-linearity of PA provides IMD3 current components dependant of bias voltage and power level. By using the properties of those currents in a two-stages amplifier, especially in term of phase, 30 dB reduction of IMD3 power level at the output of the system can be achieved. Results clearly demonstrate that the appropriate use of the non linear drain current source of driver stages can be applied to compensate output IMD in the design of multistages amplifier.

REFERENCES

[1] A. KATZ, "*SSPA Linearization*", Microwave Journal, April 1999, pp 22-42.

[2] P.B. KENINGTON, "*Methods Linearize RF Transmitters and Power Amps*" (Part 1), "Microwave & RF", vol. 37,no 13, December 1998, pp.102-116.

[3] K. YAMAUCHI, K. MORI, M. NAKAYAMA, Y. MITSUI and T. TAKAGI. "*A microwave miniaturized linearizer using a parallel diode.*" 1997 MTT-S. p1199-1202.

[4] K. YAMAUCHI, K. MORI, M. NAKAYAMA, Y. ITOH, Y.MITSUI and O.ISHIDA. "*A novel Series Diode Linearizer for Mobile Radio Power Amplifiers.*" 1996 MTT-S. p831-834.

[5] S.OGURA, K.SEINO, T.ONO, A.KAMIKOKURA and H.HIROSE. "*Development of a compact, broadband FET linearizer for satellite use.*" 1997 MTT-S,p1195-1198.

[6] N.B. de CARVALHO, J.C. PEDRO. "*Large and small signal IMD Behavior of Microwave Power Amplifiers*" IEEE Transactions On Microwave Theory and Techniques, vol 47, No 12, Dec 1999.